CSCO: A Backside-PDN-Aware Clock–Signal Co-Optimization Framework for Improved PPA

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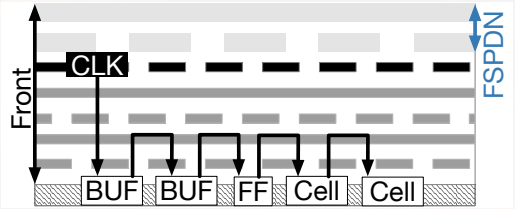
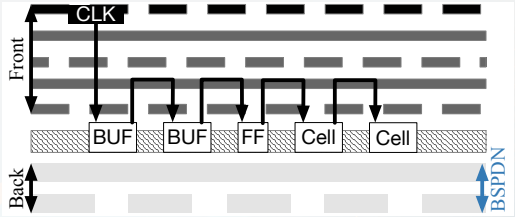
Backside power delivery

Conventional frontside PDN



Backside PDN



Moving power delivery frees frontside routing resources

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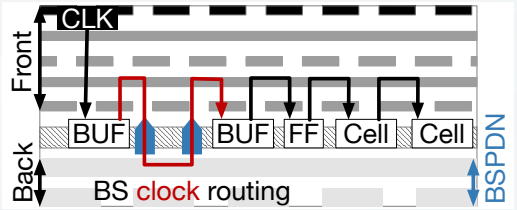
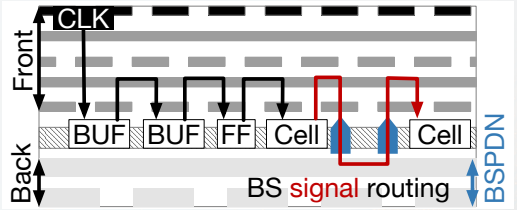
Clock and signal nets share backside capacity

Clock routing only



Signal routing only



Clock nets + Signal nets

One shared routing budget

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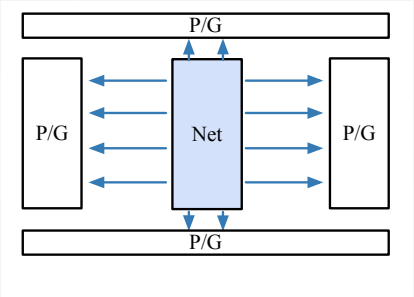
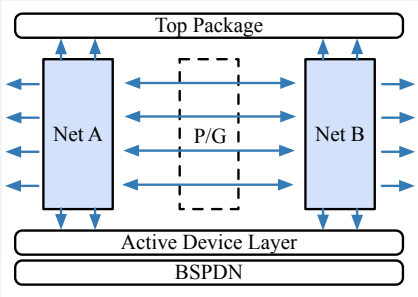
Frontside P/G removal increases coupling



Frontside P/G shielding



Direct coupling between adjacent nets

Backside adoption also creates a signal integrity problem

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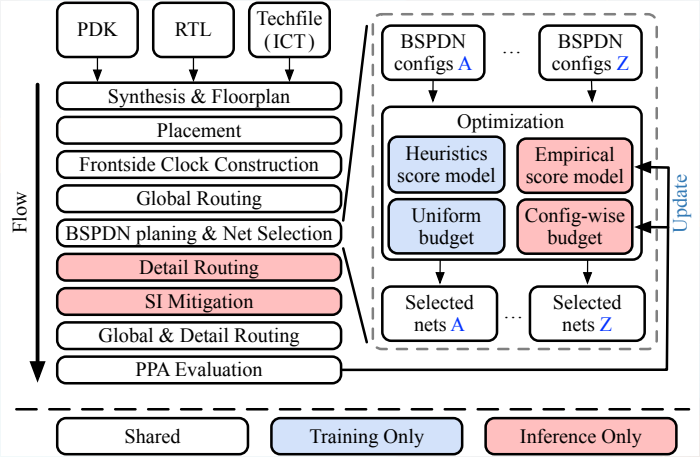
CSCO framework



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0–1 optimization problem

We model backside net assignment as a 0–1 problem.

$\mathcal{N} = \{s_1, \ldots, s_m, c_1, \ldots, c_n\}$: m signal nets, n clock nets

$x_i = 1$: net i uses the backside $\quad$ $x_i = 0$: frontside

$$\max_{\mathbf{x}} \quad \mathrm{Eval}(\mathbf{x}) = T_{\mathrm{wns}}(\mathbf{x}) + \lambda\, T_{\mathrm{tns}}(\mathbf{x})$$

$$\text{s.t.} \quad x_i \in \{0, 1\}, \quad i = 1, \ldots, m+n.$$

What physical constraints must this allocation satisfy?

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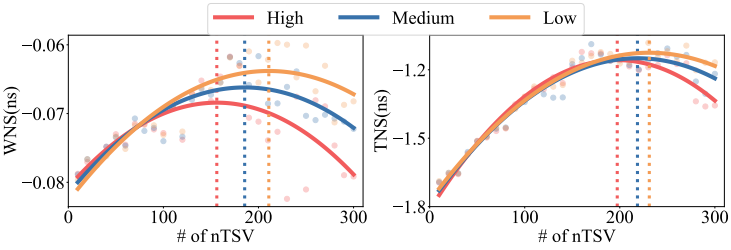
PDN-dependent nTSV budget

Observation: timing gains peak at PDN-dependent nTSV counts.



Timing turning points set B for each PDN t_i: nTSV cost (pin count)

$$\sum_{i=1}^{m+n} t_i x_i \;\leq\; B(\text{PDN configuration})$$

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Timing surrogate

Full routing and timing analysis make direct search expensive.

Predict timing for a complete clock–signal allocation $\mathbf{x}$:

$$\widehat{y}(\mathbf{x}) \approx \mathrm{Eval}(\mathbf{x}) = T_{\mathrm{wns}}(\mathbf{x}) + \lambda\, T_{\mathrm{tns}}(\mathbf{x})$$

Use the learned estimate during net-allocation search:

$$\begin{aligned} \max_{\mathbf{x}} \quad & \widehat{y}(\mathbf{x}) \\ \text{s.t.} \quad & \sum_i t_i x_i \le B, \quad \mathbf{x} \in \{0,1\}^{m+n}. \end{aligned}$$

How can we learn net interactions from limited labels?

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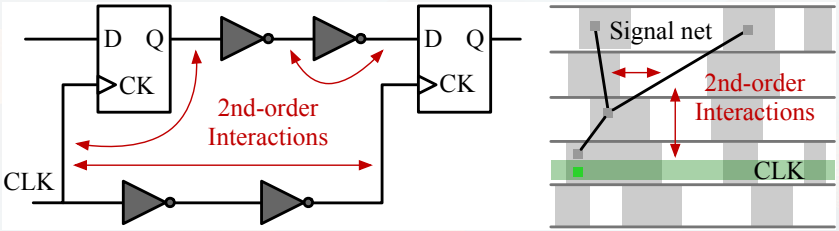
Second-order factorization machine

Pairwise timing dependencies motivate a second-order model.



$$\hat{y}(\mathbf{x}) = w_0 + \mathbf{w}^\mathsf{T}\mathbf{x} + \sum_{i<j} \langle \mathbf{v}_i, \mathbf{v}_j \rangle x_i x_j$$

Low-rank embeddings $\mathbf{v}_i \in \mathbb{R}^l$ share parameters across net pairs

How do we obtain the training allocations?

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Cold-start data construction

Cold-start data should cover useful and diverse allocations.

Symbol (unit)	Definition	Range	Net type
$\tilde{t}_{\text{tran}}$ (ps)	Transition delay	≥ 0	Both
$\tilde{r}_{\text{first}}$ (N/A)	Rank of first critical path	$\{1, \ldots, m+n\}$	Both
$\tilde{n}_{\text{load}}$ (N/A)	Number of loads	$\mathbb{Z}^+$	Both
$\tilde{C}_{\text{est}}$ (fF)	Estimated net capacitance	≥ 0	Signal
$\tilde{N}_{\text{path}}$ (N/A)	Occurrence count in all paths	$\{1, \ldots, m+n\}$	Signal
$\tilde{t}_{\text{arr}}$ (ns)	Arrival time	≥ 0	Clock
$\tilde{N}_{\text{crit}}$ (N/A)	Occurrences in top-200 critical paths	$\{0, \ldots, 200\}$	Clock

Prioritize timing potential per nTSV. Random replacement adds diversity.

How do these allocations become training labels?

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Physical labels and FM training

Surrogate learning requires physically evaluated allocations.

Detailed routing and signoff supply the label for each allocation:

$$\mathcal{D} = \{(\mathbf{x}^{(r)}, y^{(r)})\}_{r=1}^{S}, \qquad y^{(r)} = \mathrm{Eval}(\mathbf{x}^{(r)})$$

Fit the FM to allocation–timing pairs using mean squared error:

$$\min_{\theta} \frac{1}{S} \sum_{r=1}^{S} \left(\widehat{y}_{\theta}(\mathbf{x}^{(r)}) - y^{(r)} \right)^2$$

SGD learns the FM parameters $\theta = \{w_0, \mathbf{w}, \mathbf{V}\}$

How does the trained FM guide net selection?

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FM-guided net selection

Each selected net must justify its nTSV cost.

FM-guided greedy seed

$$I_i(\mathbf{x}) = \frac{w_i + \sum_{j \neq i} \langle \mathbf{v}_i, \mathbf{v}_j \rangle x_j}{t_i}$$

Predicted timing benefit per nTSV under the clock/signal budgets

Simulated annealing explores better net combinations

$$P_{\text{accept}} = \min\left(1, \exp\left(\frac{\widehat{y}(\mathbf{x}') - \widehat{y}(\mathbf{x})}{T}\right)\right)$$

$\mathbf{x}'$: a feasible swap T: temperature that cools during search

What SI risks remain after timing optimization?

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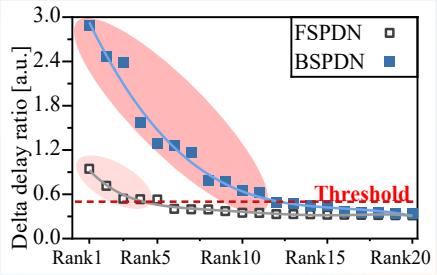
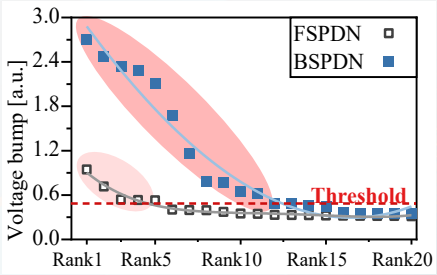
Signal integrity after net selection

Timing optimization does not directly constrain local crosstalk.





4 GHz comparison: SI penalties concentrate in a small subset of nets

How should we repair the most vulnerable nets?

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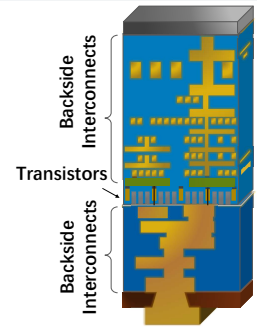
SI-aware backside refinement

Backside power metals can shield SI-critical nets.



1. Identify SI-critical nets
Inspect post-route delta delay and voltage bump

2. Rank and reassign
Move severe nets to reserved backside tracks

3. Re-route and verify
Run timing and SI signoff on the updated routing

Final routing and signoff evaluate both timing and SI

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Experimental setup

Which designs and baselines are compared?

7 nm 0.75 V 2 GHz target

Design	Signal nets	Clock nets
SHA256	7.8k	172
JPEG	180k	3.5k
Cortex-A7	116k	1.5k

Genus / Innovus implementation
PrimeTime SI timing signoff
In-house IR-drop evaluation

Method	Routing / PDN setting
FS	Frontside PDN and routing
BSPDN+FR	Backside PDN, frontside routing
DAC24	GNN-based backside clock assignment
DAC25	Critical-path backside clock routing
CSCO	**Joint clock–signal selection**

CSCO clock / signal budget split: **30% / 70%**

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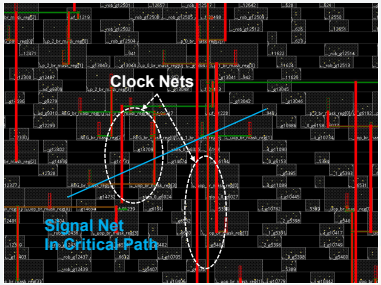
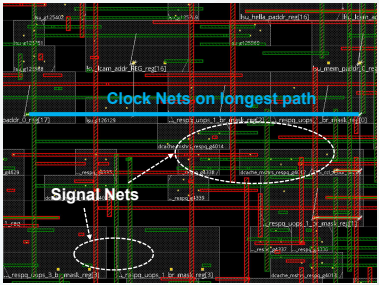
Critical signal and clock routes

Frontside congestion limits critical signal and clock routing



(a) Signal net on a critical path



(b) Clock net on a maximum-latency path

Does joint backside allocation improve endpoint timing?

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Timing comparison

Does joint clock–signal selection improve timing?

SHA256	FS	BSPDN+FR	DAC24	DAC25	**CSCO**
WNS (ns)	-0.196	-0.111	-0.094	-0.106	**-0.061**
TNS (ns)	-4.06	-1.96	-2.04	-2.14	**-1.09**
Eff. freq. (GHz)	1.50	1.64	1.70	1.65	**1.78**
JPEG	FS	BSPDN+FR	DAC24	DAC25	**CSCO**
WNS (ns)	-0.150	-0.126	-0.122	-0.125	**-0.077**
TNS (ns)	-28.53	-25.25	-24.44	-25.06	**-7.66**
Eff. freq. (GHz)	1.54	1.61	1.63	1.60	**1.73**
Cortex-A7	FS	BSPDN+FR	DAC24	DAC25	**CSCO**
WNS (ns)	-0.194	-0.081	-0.092	-0.106	**-0.011**
TNS (ns)	-1.756	-1.637	-1.579	-1.499	**-1.139**
Eff. freq. (GHz)	1.44	1.72	1.69	1.65	**1.96**

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Resource and power trade-offs

What are the nTSV, power, and IR-drop costs?

SHA256	FS	BSPDN+FR	DAC24	DAC25	**CSCO**
#nTSV	N/A	N/A	270	194	230
Total power (mW)	7.41	7.17	6.77	7.09	7.05
IR-drop (mV)	62.54	14.13	14.32	14.25	14.35
JPEG	FS	BSPDN+FR	DAC24	DAC25	**CSCO**
#nTSV	N/A	N/A	396	768	800
Total power (mW)	152.92	143.42	149.01	137.44	140.21
IR-drop (mV)	55.95	23.79	24.09	24.02	25.99
Cortex-A7	FS	BSPDN+FR	DAC24	DAC25	**CSCO**
#nTSV	N/A	N/A	316	634	600
Total power (mW)	140.97	131.93	122.67	120.01	142.68
IR-drop (mV)	170.02	17.88	18.93	18.03	18.58

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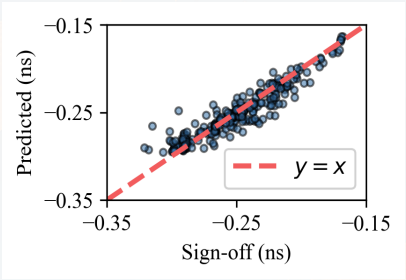
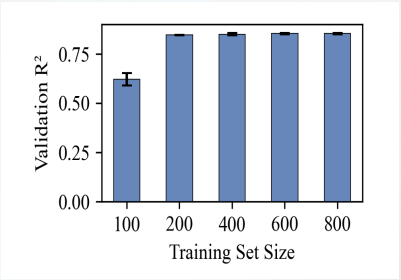
Surrogate validation

Can a small training set support accurate prediction?





$R^2 = 0.858$ **RMSE 14.1 ps**

337 held-out SHA256 allocations

200 training allocations for SHA256

Three-run mean and standard deviation

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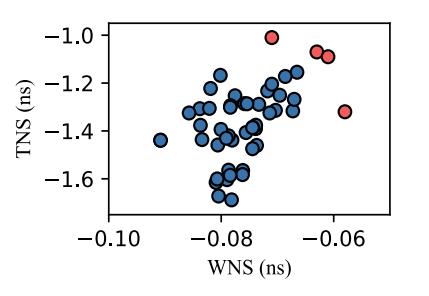
Search quality and evaluation cost

Does fast surrogate evaluation find better allocations?



Training (blue) and inference (red) solutions
Larger WNS and TNS are better

Per-candidate evaluation

323.4 s
PrimeTime signoff

< 0.03 **s**
FM evaluation

Excludes data collection
and final routing

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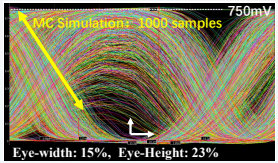
Signal integrity and eye opening

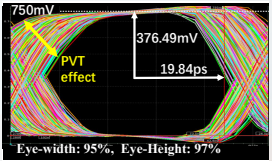
Does SI refinement reduce violations across designs?

Design	FS Delay	FS Bump	BSPDN+FR Delay	BSPDN+FR Bump	**CSCO** Delay	**CSCO** Bump
SHA256	3	1	8	3	**2**	**0**
JPEG	3	2	16	12	**4**	**2**
Cortex-A7	7	5	17	27	**2**	**3**

Violations: $r_{\text{delay}} > 0.4$, $r_{\text{bump}} > 0.3$. Eyes: one worst-case net.



Frontside routing



Double-sided routing

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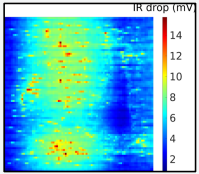
PDN-dependent timing and power integrity

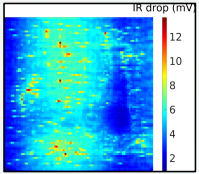
How does the power grid change the routing trade-off?

SHA256: increasing power-stripe width, with pitch fixed

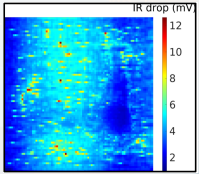
Config.	IR-drop (mV)	#nTSV	WNS (ns)	TNS (ns)
BSPDN-1	15.76	240	-0.060	-1.17
BSPDN-2	14.35	230	-0.061	-1.09
BSPDN-3	13.61	210	-0.067	-1.18



BSPDN-1



BSPDN-2



BSPDN-3

Original per-map color scales. Compare the IR-drop values in the table.

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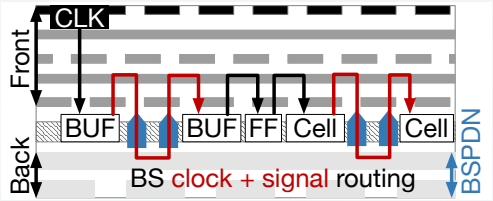
Takeaways



Joint clock–signal selection
under a PDN-dependent budget

Compact timing surrogate
for fast candidate evaluation

Backside shielding for SI
with reserved routing resources

+36.1% frequency on Cortex-A7 **80.5% / 88.1% fewer SI violations**

Frequency vs. FS. Delay / bump reductions vs. BSPDN+FR, summed over three designs.

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Thanks

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Backup topics

Topic	Pages
Allocation and empirical cold-start	B2, B3
Training and inference parameters	B4
Backside technology and extraction	B5
SI definitions and critical-net results	B6, B7
PDN routing and configuration tables	B8, B9
Complete benchmark comparisons	B10, B11, B12
Evaluation scope	B13

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Allocation objective and routing budget

How is backside capacity enforced?

$$\max_{\mathbf{x}} \quad T_{\mathrm{WNS}}(\mathbf{x}) + 0.1\, T_{\mathrm{TNS}}(\mathbf{x})$$

$$\text{s.t.} \quad \sum_{i=1}^{m+n} t_i x_i \le B, \qquad x_i \in \{0,1\}.$$

$x_i = 1$	Assign net i to the backside.
t_i	Required nTSVs, equal to the net's pin count.
B	Empirical timing–nTSV turning point for a PDN configuration.
Budget split	Clock / signal: **30% / 70%** in the reported experiments.

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Empirical cold-start scoring

What guides sampling before the FM is trained?

$$\begin{aligned}\mathrm{Score}_{\mathrm{sig}} = \alpha_1 \tilde{t}_{\mathrm{tran}} + \alpha_2 \tilde{n}_{\mathrm{load}} + \alpha_3 \tilde{C}_{\mathrm{est}} \\ + \alpha_4 \tilde{N}_{\mathrm{path}} - \alpha_5 \tilde{r}_{\mathrm{first}},\end{aligned}$$

$$\begin{aligned}\mathrm{Score}_{\mathrm{clk}} = \beta_1 \tilde{t}_{\mathrm{tran}} + \beta_2 \tilde{n}_{\mathrm{load}} + \beta_3 \tilde{N}_{\mathrm{crit}} \\ - \beta_4 \tilde{t}_{\mathrm{arr}} - \beta_5 \tilde{r}_{\mathrm{first}}.\end{aligned}$$

Normalize metrics to $[0, 1]$ and use equal weights.

Rank by Score_i / t_i, then replace 20% of selected nets for exploration.

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Training and inference parameters

Which settings are used in the reported experiments?

FM training	Setting
Embedding dimension	12
Loss / optimizer	MSE / SGD
Batch size	32
Learning rate	10^{-4}
Update steps	5,000
Samples: SHA256	200
Samples: JPEG / Cortex-A7	500 each

Sampling / search	Setting
Exploration replacement	20%
SA initial temperature	10^{-5}
SA cooling factor	0.995
SA stopping temperature	10^{-6}
Clock / signal budget	30% / 70%

FM training: within 15 minutes on one GPU.

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Backside interconnect technology

How does the flow model backside interconnects?

BS	Width/spacing (μm)	Pitch (μm)	FS	Width/spacing (μm)	Pitch (μm)
BSM0	0.053 / 0.028	0.04	M0	0.020 / 0.020	0.04
BSM1	0.125 / 0.375	0.5	M1	0.037 / 0.020	0.06
BSM2	0.5 / 1.5	2	M2/3	0.020 / 0.020	0.04
BSM3	0.5 / 1.5	2	M4–M8	0.038 / 0.038	0.08

Custom ICT / QRC files define the backside stack and extraction.

TCAD nTSV model: $C_{\mathrm{nTSV}} = 0.444\,\mathrm{fF}$, $R_{\mathrm{nTSV}} = 23\,\Omega$.

Frontside / backside parasitics are merged for timing signoff.

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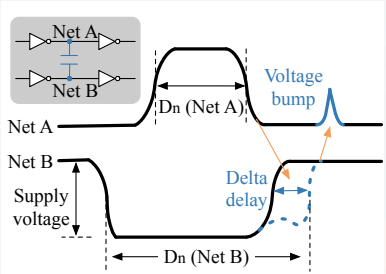
Signal integrity metrics and thresholds

Which thresholds define the reported SI counts?



$$r_{\text{delay}} = \frac{\Delta D}{D_d + D_n + \Delta D}, \qquad r_{\text{bump}} = \frac{V_{\text{bump}}}{V_{\text{DD}}}.$$

Criterion	Delay ratio	Bump ratio
SI-critical flag	> 0.4	> 0.4
Reported violation	> 0.4	> 0.3

Either ratio can trigger the SI-critical flag.

D_d: driver delay. D_n: net delay.

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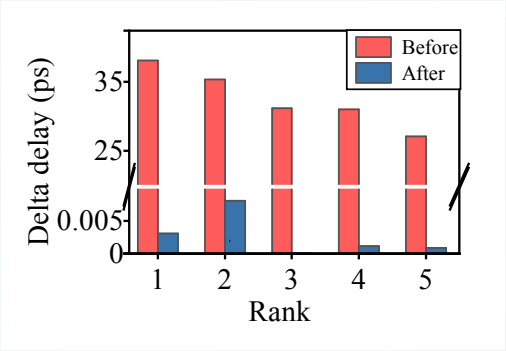
SI delay on five critical nets

How does refinement change the most vulnerable nets?



Before / after SI refinement. The original figure uses a broken vertical axis.

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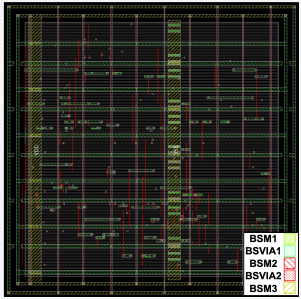
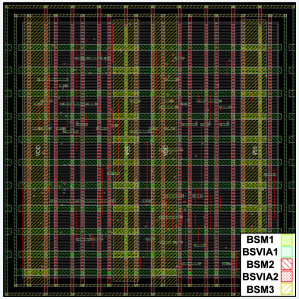
Backside routing under different power grids

How does PDN density change routing patterns?



BSPDN-1: sparse grid



BSPDN-3: dense grid

SHA256. Wider power stripes reduce the space available for net routing.

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Power-rail configurations and complete results

SHA256. Rail parameters list BSM1 / BSM2 / BSM3 values.

BSM1 / BSM2 / BSM3	BSPDN-1	BSPDN-2	BSPDN-3
Rail width (μm)	0.10/0.40/1.0	0.20/0.60/2.0	0.35/0.80/3.0
Rail pitch (μm)	2.1/1.8/10	2.1/1.8/10	2.1/1.8/10
Unit r (Ω/μm)	4.20/0.21/0.016	1.86/0.14/0.008	1.10/0.10/0.005
Unit c (fF/μm)	0.41/0.23/0.083	0.37/0.21/0.153	0.39/0.30/0.270

Config.	IR-drop (mV)	#nTSV	WNS (ns)	TNS (ns)	Delay	Bump
BSPDN-1	15.76	240	-0.060	-1.17	2	1
BSPDN-2	14.35	230	-0.061	-1.09	2	0
BSPDN-3	13.61	210	-0.067	-1.18	1	1

Delay / bump counts use $r_{\mathrm{delay}} > 0.4$ / $r_{\mathrm{bump}} > 0.3$.

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Full results: SHA256

Metric	FS	BSPDN+FR	DAC24	DAC25	**CSCO**
Utilization (%)	82.91	82.36	82.36	82.36	82.36
Area (μm^2)	1319	1311	1311	1311	1311
Metal layers (BS+FS)	0+6	3+6	3+6	3+6	3+6
nTSVs	N/A	N/A	270	194	230
Clock skew (ps)	24.17	27.94	27.02	19.72	32.09
Clock latency (ps)	83.29	75.31	64.63	51.47	75.13
Wirelength (m)	0.05	0.04	0.04	0.04	0.04
Power (mW)	7.41	7.17	6.77	7.09	7.05
IR-drop (mV)	62.54	14.13	14.32	14.25	14.35
WNS (ns)	-0.196	-0.111	-0.094	-0.106	**-0.061**
TNS (ns)	-4.06	-1.96	-2.04	-2.14	**-1.09**
Effective frequency (GHz)	1.50	1.64	1.70	1.65	**1.78**
Delay violations	3	8	8	8	**2**
Bump violations	1	3	3	3	**0**

2 GHz target. SI counts: delay ratio > 0.4, bump ratio > 0.3.

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Full results: JPEG

Metric	FS	BSPDN+FR	DAC24	DAC25	**CSCO**
Utilization (%)	78.24	75.50	75.50	75.50	75.50
Area (μm^2)	31285	32280	32280	32280	32280
Metal layers (BS+FS)	0+7	3+7	3+7	3+7	3+7
nTSVs	N/A	N/A	396	768	800
Clock skew (ps)	112.16	35.37	31.93	24.86	34.17
Clock latency (ps)	226.26	149.31	112.11	79.31	124.46
Wirelength (m)	0.81	0.70	0.69	0.68	0.69
Power (mW)	152.92	143.42	149.01	137.44	140.21
IR-drop (mV)	55.95	23.79	24.09	24.02	25.99
WNS (ns)	-0.150	-0.126	-0.122	-0.125	**-0.077**
TNS (ns)	-28.53	-25.25	-24.44	-25.06	**-7.66**
Effective frequency (GHz)	1.54	1.61	1.63	1.60	**1.73**
Delay violations	3	16	16	16	**4**
Bump violations	2	12	12	12	**2**

2 GHz target. SI counts: delay ratio > 0.4, bump ratio > 0.3.

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Full results: Cortex-A7

Metric	FS	BSPDN+FR	DAC24	DAC25	**CSCO**
Utilization (%)	78.16	74.15	74.15	74.15	74.15
Area (μm^2)	14267	13491	13491	13491	13491
Metal layers (BS+FS)	0+8	3+8	3+8	3+8	3+8
nTSVs	N/A	N/A	316	634	600
Clock skew (ps)	217.67	95.06	66.79	52.97	43.49
Clock latency (ps)	456.98	206.51	147.67	123.87	135.80
Wirelength (m)	1.47	1.37	1.38	1.38	1.39
Power (mW)	140.97	131.93	122.67	120.01	142.68
IR-drop (mV)	170.02	17.88	18.93	18.03	18.58
WNS (ns)	-0.194	-0.081	-0.092	-0.106	**-0.011**
TNS (ns)	-1.756	-1.637	-1.579	-1.499	**-1.139**
Effective frequency (GHz)	1.44	1.72	1.69	1.65	**1.96**
Delay violations	7	17	17	17	**2**
Bump violations	5	27	26	27	**3**

2 GHz target. SI counts: delay ratio > 0.4, bump ratio > 0.3.

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Evaluation scope

What do the reported comparisons establish?

Topic	Scope of the evidence
Budget ratio	Clock / signal split is fixed at 30% / 70%.
Model reuse	Across PDN configurations within a design.
Evaluation cost	323.4 s vs. < 0.03 s per candidate. Data collection and final implementation are excluded.
Timing and power	WNS < 0 at 2 GHz. Power / resource trade-offs remain.
References	Frequency gain compares with FS. SI reductions compare with BSPDN+FR, summed over three designs.

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